BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,886	02/22/2002	Vicente V. Cavanna	10011175	9403

7590 07/28/2004

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. box 7599
Loveland, CO 80537-0599

EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/080,886	CAVANNA ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *7-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 15-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20040722*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-6 and 15-17, drawn to A Method for Adjusting an m-Bit CRC of a Sub-Message Comprising the Steps of Examining Each Bit of N, where N Equals n Mod (2.sup.m-1), in order from the Most Significant Bit to the Least Significant Bit; the Examining Act for Each Examined Bit Comprising: Finite Field Squaring the Contents of the m-Bit Memory Location, classified in class 714, subclass 781.

II. Claims 7-10, drawn to A Method for Adjusting an m-Bit CRC of a Sub-Message Comprising the Steps Computing $Y=x^n$ mod P(x) Using a Lookup Table; and Field Multiplying the Partial m-Bit CRC and Y Together, classified in class 714, subclass 759.

III. Claims 11-14, drawn to A Method of Adjusting a CRC of a Message Composed of a Plurality of Sub-Messages wherein the Adjustment is in Response to Changes in a Given Sub-Message Comprising the Steps of Storing a Second m-Bit CRC in a First m-Bit Memory Location; Examining Each Bit of N in Order from the Most Significant Bit to the Least Significant Bit; the Examining Act for Each Examined Bit Comprising: Finite Field Squaring the Contents of the Second m-Bit Memory Location, classified in class 714, subclass 781.

The inventions are distinct, each from the other because of the following reasons: Inventions Group I; A Method for Adjusting an m-Bit CRC of a Sub-Message Comprising the Steps of Examining Each Bit of N, where N Equals n Mod (2.sup.m-1), in order from the Most Significant Bit to the Least Significant Bit; the Examining Act for Each Examined Bit Comprising: Finite Field Squaring the Contents of the m-Bit Memory Location; and Group II; A Method for Adjusting an m-Bit CRC of a Sub-Message Comprising the Steps Computing $Y=x^n$ mod P(x) Using a Lookup Table; and Field Multiplying the Partial m-Bit CRC and Y Together; are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I; A Method for Adjusting an m-Bit CRC of a Sub-Message Comprising the Steps of Examining Each Bit of N, where N Equals n Mod (2.sup.m-1), in order from the Most Significant Bit to the Least Significant Bit; the Examining Act for Each Examined Bit Comprising: Finite Field Squaring the Contents of the m-Bit Memory Location; has separate utility such as in a device using arithmetic units for performing all calculations. In the instant case, invention Group II; A Method for Adjusting an m-Bit CRC of a Sub-Message Comprising the Steps Computing $Y=x^n$ mod P(x) Using a Lookup Table; and Field Multiplying the Partial m-Bit CRC and Y Together; has separate utility such as using lookup tables in place of calculators for arithmetic calculations. See MPEP § 806.05(d).

Inventions Group I; A Method for Adjusting an m-Bit CRC of a Sub-Message Comprising the Steps of Examining Each Bit of N, where N Equals n Mod (2.sup.m-1), in order from the Most Significant Bit to the Least Significant Bit; the Examining Act for Each Examined Bit Comprising: Finite Field Squaring the Contents of the m-Bit Memory Location; and Group III; A Method of Adjusting a CRC of a Message Composed of a Plurality of Sub-Messages wherein the Adjustment is in Response to Changes in a Given Sub-Message Comprising the Steps of Storing a Second m-Bit CRC in a First m-Bit Memory Location; Examining Each Bit of N in Order from the Most Significant Bit to the Least Significant Bit; the Examining Act for Each Examined Bit Comprising: Finite Field Squaring the Contents of the Second m-Bit Memory Location; are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I; A Method for Adjusting an m-Bit CRC of a Sub-Message Comprising the Steps of Examining Each Bit of N, where N Equals n Mod (2.sup.m-1), in order from the Most Significant Bit to the Least Significant Bit; the Examining Act for Each Examined Bit Comprising: Finite Field Squaring the Contents of the m-Bit Memory Location; has separate utility such as for delaying CRC data. In the instant case, invention Group III; A Method of Adjusting a CRC of a Message Composed of a Plurality of Sub-Messages wherein the Adjustment is in Response to Changes in a Given Sub-Message Comprising the Steps of Storing a Second m-Bit CRC in a First m-Bit Memory Location; Examining Each Bit of N in Order from the Most Significant Bit to the Least Significant Bit; the Examining Act for Each Examined Bit

Comprising: Finite Field Squaring the Contents of the Second m-Bit Memory Location; has separate utility such as adjusting a CRC of a message composed of a plurality of sub-messages wherein the adjustment is in response to changes in a given sub-message. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Groups II & III and vice a versa, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Pamela Kee on 12 July 2004 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-6 and 15-17. Affirmation of this election must be made by applicant in replying to this Office action. Claims 7-10 and 11-14 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-6 and 15-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the CRC generating polynomial" in lines 1 and 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites, "examining each bit of N, where N equals n mod (2^{m-1})", which makes no sense since it is not clear how a bit can relate to a number N.

Claim 1 recites the limitation "the most significant bit" in lines 5 and 6. There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites the limitation "the least significant bit" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites the limitation "the next state" in line 10. There is insufficient antecedent basis for this limitation in the claim.

The variables n, m and N in claim 1 are undefined.

Claim 5 recites the limitation " m-bit CRC is equal or congruent to one" in lines 2 and 3, which makes no sense since an m-bit CRC is an m-bit vector and not a number.

Claim 5 recites, "examining each bit of N, where N equals n mod (2^{m-1})", which makes no sense since it is not clear how a bit can relate to a number N.

Claim 5 recites the limitation "the most significant bit" in lines 5 and 6. There is insufficient antecedent basis for this limitation in the claim.

Claim 5 recites the limitation "the least significant bit" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim 5 recites the limitation "the next state" in line 10. There is insufficient antecedent basis for this limitation in the claim.

The variables n, m and N in claim 5 are undefined.

Claim 15 recites, "examining each bit of N, where N equals n mod (2^{m-1})", which makes no sense since it is not clear how a bit can relate to a number N.

Claim 15 recites the limitation "the most significant bit" in lines 4 and 5. There is insufficient antecedent basis for this limitation in the claim.

Claim 15 recites the limitation "the least significant bit" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim 5 recites the limitation "the next state" in line 9. There is insufficient antecedent basis for this limitation in the claim.

The variables n, m and N in claim 15 are undefined.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Burshtein; David (US 6038577 A).

35 U.S.C. 102(b) rejection of claim 15.

Burshtein teaches storing an m-bit polynomial in an m-bit memory location (the LFSR in Figure 4 is an m-bit storage device for); examining each bit of N, where N equals n mod 2^{m-1} (N = q = n in Figure 5; Note: each bit q_i of the binary representation of q is examined), in order from the most significant bit to the least significant bit (The binary representation of q in Figure 5 of Burshtein is examined by looping over i = 1,...,l-1 for each bit q_i of q; Note: q = q mod 2^{m-1} since l <= m in equation 12 in column 6 of Burshtein; Note also looping in the order of the most significant bit to the least significant is encompassed by Burshtein and is a particular embodiment of the looping in Figure 5 of Burshtein); the examining act for each examined bit comprising: finite field squaring the contents of the m-bit memory location (step 96 in Figure 5 of Burshtein), and; if the examined bit equals one (step 98 in Figure 5 of Burshtein), advancing the

contents of the m-bit memory location to the next state as determined by the Galois field defined by the CRC generating polynomial (step 100 in Figure 5 of Burshtein: Note: the m-bit storage register of Figure 5 is defined by a CRC generating polynomial).

35 U.S.C. 102(b) rejection of claims 16 and 17.

Generator polynomials for an LFSR are either primitive polynomials that are irreducible or are comprised of primitive polynomials (Note: if the generator polynomial is made up of primitive or irreducible factors, it is not primitive or irreducible).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burshtein; David (US 6038577 A).

35 U.S.C. 103(a) rejection of claims 1 and 5.

Burshtein teaches storing an m-bit polynomial in an m-bit memory location (the LFSR in Figure 4 is an m-bit storage device for); examining each bit of N, where N equals n mod 2^{m-1} (N = q = n in Figure 5; Note: each bit q_i of the binary representation of q is examined), in order from the most significant bit to the least significant bit (The binary representation of q in Figure 5 of Burshtein is examined by looping over i = 1,...,l-1 for each bit q_i of q; Note: q = q mod 2^{m-1} since l <= m in equation 12 in column 6 of Burshtein; Note also looping in the order of the most significant bit to the least significant is encompassed by Burshtein and is a particular embodiment of the looping in Figure 5 of Burshtein); the examining act for each examined bit comprising: finite field squaring the contents of the m-bit memory location (step 96 in Figure 5 of Burshtein), and; if the examined bit equals one (step 98 in Figure 5 of Burshtein), advancing the contents of the m-bit memory location to the next state as determined by the Galois field defined by the CRC generating polynomial (step 100 in Figure 5 of Burshtein: Note: the m-bit storage register of Figure 5 is defined by a CRC generating polynomial). However Burshtein does not explicitly teach that $a_0,...a_{m-1}$ in Figure 5 is an m-bit CRC. The Examiner asserts that the LFSR in Figure 5 of Burshtein is used for delaying an m-bit data stream. The Examiner asserts that that the CRC bits $a_0,...a_{m-1}$ of a systematic CRC code $c_0,...c_N$ for an information stream $i_0,...i_k$ is generally arranged whereby $i_0=c_0$, $i_1-c_1,...$, $i_k=c_k$ the CRC bit are delayed so that $a_0=c_{k+1}$, $a_1-c_{k+2},...$, $a_k=c_N$

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Burshtein by including use of the delay device of Figure 5 for CRC data. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the delay device of Figure 5 for CRC data would have provided the opportunity to create a systematic code.

35 U.S.C. 103(a) rejection of claims 2, 3 and 6.

Generator polynomials for an LFSR are either primitive polynomials that are irreducible or are comprised of primitive polynomials (Note: if the generator polynomial is made up of primitive or irreducible factors, it is not primitive or irreducible).

35 U.S.C. 103(a) rejection of claim 4.

The algorithm of Figure 5 in Burshtein performs finite field squaring act and the advancing the contents act substantially, simultaneously, in the same cycle.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133